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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,517	02/28/2002	Douglas J. Vanesko	CISCP716	2156

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EXAMINER	
TSEGAYE, SABA	

ART UNIT	PAPER NUMBER
2616	

DATE MAILED: 08/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,517	VANESKO, DOUGLAS J.	
	Examiner	Art Unit	
	Saba Tsegaye	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-9 and 11-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-9, and 11-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the amendment filed 05/24/06. Claims 1, 3-9, and 11-22 are pending. Currently no claims are in condition for allowance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 3-9, and 11-22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 9, and 19:

The phrases "*mapping links for signals between nodes is selected to* ***minimize*** *the differences between the number of links between each of the input nodes and center nodes and the differences between the number of links between each of the center nodes and output nodes*" and "*mapping links for signals between nodes is selected to* ***minimize*** *the differences between the number of links between the nodes*" do not clearly describe Figs. 6B-6C. These phrases are confusing. Since it does not appear that there is any minimization taken place in term of the total input links of each node and the total output links of each node.

Claim 21:

Line 5, the phrase "the number of signals" lack antecedent basis.

Line 8, the phrase "the number of signals" lack antecedent basis.

Claim Rejections - 35 USC § 102

4. Claim 21 is rejected under 35 U.S.C. 102(e) as being anticipated by Kam et al. (US 2002/0146003 A1).

Kam discloses, in figs. 2, 2A, and 3, a method of mapping signals across a network element switch having a plurality of input nodes (202), a plurality of center nodes (204) and a plurality of output nodes (206) comprising:

for each possible mapping of a specific signal across the network element switch, calculating the number of signals between each of the input nodes and center nodes (0011; 0037);

for each possible mapping of the specific signal across the network element switch, calculating the number of signals between each of the center nodes and output nodes (0011; 0023; 0042); and

selecting the mapping of the specific signal across the network element switch where the difference in the number of signals between each of the input nodes and center nodes is minimized and the difference in the number of signals between each of the center nodes and output nodes is minimized (011; 0032).

Claim Rejections - 35 USC § 103

5. Claims 1, 3-9, 11-20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wolf in view of Kam et al. (US2002/0146003 A1).

Claims 1 and 9, Wolf discloses, in fig. 1, a network element switch, comprising:

a pair of input nodes (I), each input node having 2n inputs and 2n outputs, where n is greater than or equal to 1;

a pair of center nodes (II), each center node receiving n inputs from each of the input nods and having 2n outputs (see 24);

a pair of output nodes (III), each output node receiving n inputs from each of the center nodes and having 2n outputs (see 31 and 32); and

wherein an any-to-any mapping is not guaranteed from the pair of input nodes to the pair of output nodes (switching modules 21-25 are capable of splitting point-to-multipoint connections, this shows that any-to-any mapping is not guaranteed at switching modules 31-35).

Wolf does not expressly disclose mapping links for signals between nodes is selected to minimize the differences between the number links between the nodes.

Kam teaches a load-sharing algorithm that can be used **to spread the component signal** among the mid-stage switching stags (see fig. 2A; 011; 0032). Kam teaches a CLOS network is completely defined by the mid-stage switching module selected to carry the component signal. For a groomed circuit, the component signals may be routed together through the same mid-stage switching module or **alternatively**, the groomed component signals may be individually routed through a plurality of various mid-stage switching modules, via connections of varying bandwidths (see 0023)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolf system to incorporate to be able to minimize the differences between the number links between the nodes, as suggested by Kam. The motivation is to route each

component signal through the mid-stage switching module having the largest available bandwidth (see abstract).

Regarding claims 3 and 11, Wolf discloses the network element wherein n is greater than or equal to 2 (see fig. 1).

Regarding claims 4-6 and 12-14, Wolf discloses all the claim limitations as stated above. Further, Wolf discloses that the center node is multi-cast (column 3, lines 25-29) and each input node is unicast (column 2, lines 49-50) (as in claims 5 and 13). However, Wolf does not expressly disclose each output node and each input node is bi-cast.

Kam teaches, in Fig. 2, a three-stage CLOS switch network, wherein the input signals may be dualcast (see 0025).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolf apparatus to incorporate a set up where each input node and each output node could perform bi-cast. The motivation is to increase the whole switch capacity by utilizing non-blocking point-to-multipoint connections.

Regarding claims 7 and 15, Wolf discloses all the claim limitations as stated above. Further, Wolf discloses that the center node is multi-cast (column 3, lines 25-29) and each input node is unicast (column 2, lines 49-50) (as in claims 5 and 13). However, Wolf does not expressly disclose the inputs and outputs carry STS-48 signal.

Kam teaches in Fig. 2, a three-stage 2N CLOS switch network that receives a plurality of inputs of OC-N signals such as OC-48 (see 0025).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolf apparatus to incorporate where the inputs and outputs carry STS-48 signal in order to provide a higher rate signals.

Regarding claims 8 and 16, Wolf discloses all the claim limitations as stated above. Further, Wolf discloses that the center node is multi-cast (column 3, lines 25-29) and each input node is unicast (column 2, lines 49-50) (as in claims 5 and 13). However, Wolf does not expressly disclose each node is a 2N Clos matrix.

Kam teaches, in Fig. 2, a three-stage 2N CLOS switch network (see 0008).
It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolf apparatus to incorporate a 2N Clos matrix, as suggested by Kam. The motivation is to insure non-blockage connections between the input ports and the output ports.

Regarding claims 17 and 19, Wolf discloses all the claim limitations as stated above, except for mapping links for signals between nodes is selected to minimize the differences between the number links between the nodes.

Kam teaches a load-sharing algorithm that can be used **to spread the component signal** among the mid-stage switching stags (see fig. 2A; 011; 0032).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Wolf system to incorporate to be able to minimize the differences between

the number links between the nodes, as suggested by Kam. The motivation is to route each component signal through the mid-stage switching module having the largest available bandwidth (see abstract).

Regarding claims 18, 20 and 22 Wolf discloses the network element switch wherein an any-to-any mapping is not guaranteed from the pair of input nodes to the pair of output nodes (switching modules 21-25 are capable of splitting point-to-multipoint connections, this shows that any-to-any mapping is not guaranteed at switching modules 31-35).

Response to Arguments

6. Applicant's arguments with respect to claims 1, 3-9, and 11-22 have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that Kam et al. does not teach selecting mappings links for signals between nodes to minimize the differences between the numbers of links between nodes. Examiner respectfully disagrees with Applicant contention. Kim clearly discloses a multistage CLOSE network that provides for non-blocking routing of one or more groomed input circuits. Non-blocking operation allows any of its inputs to be connected to any of its outputs in minimum fashion.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saba Tsegaye whose telephone number is (571) 272-3091. The examiner can normally be reached on Monday-Friday (7:30-5:00), First Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on (571) 272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ST
August 16, 2006

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